CLAIMS

What is claimed is:

1. A method of planarizing a metal layer on a semiconductor substrate, the method comprising:

forming a trench or via in a dielectric layer of the semiconductor substrate;

forming the metal layer on the dielectric layer such that the metal layer at least fills the trenches or vias;

immersing the substrate in an electrolyte plating solution having organic additives, the organic additives comprising at least one of plating accelerators, plating suppressors, and plating levelers; and

removing the excess portions of the metal layer by performing sequentially electropolishing followed by electroplating.

2. The method as recited in claim 1, wherein removing the excess portions of the metal layer further comprises a relaxation step after the electropolishing and electrolytic plating steps.

3. The method as recited in claim 1 wherein the concentrations of the organic additives are selected such that the plating rate is greater than the electropolishing rate in a topography dependant fashion.

4. The method as recited in claim 1 wherein the topography dependant fashion comprises increasing the rate of plating at corners of trenches or vias.

5. The method as recited in claim 1 wherein the removal rate of electropolishing is controlled to be equal to that of the electroplating when the polishing exposes the substrate.

6. The method as recited in claim 1 wherein the removal rate of electropolishing is controlled by one of adjusting the voltage applied to the electrodes in the electrolytic solution and the duration of the applied voltage.

7. The method as recited in claim 2 wherein the polishing, plating, and relaxation operations comprise one cycle of a pass and wherein the method comprises at least two passes performed sequentially.

8. The method as recited in claim 7 wherein the ratio of the electropolishing to electroplating rates in the first of the at least two passes is about 1.5 and the ratio of the of the electropolishing to electroplating rates in the last of the at least two passes is about 1.

9. The method as recited in claim 7 wherein the ratio of the electropolishing to plating rates in the first of the at least two passes is about 1.5 and the ratio of the of the electropolishing to electroplating rates in the last of the at least two passes is about 1, wherein the electropolishing to electroplating rates progressively decreases from the first to the last of the at least two passes.

10. The method as recited in claim 1 wherein the organic additives comprises a plating accelerator having a concentration in the electrolyte in the range from 1 to 10 ml/liter.

11. The method as recited in claim 1 wherein the organic additives comprises a plating suppressor having a concentration in the electrolyte in the range from 5 to 15 ml/liter.

12. The method as recited in claim 1 wherein the organic additives comprises a plating leveler having a concentration in the electrolyte in the range from 1 to 5 ml/liter.

13. The method as recited in claim 1 wherein the organic additives comprises a plating accelerator having a concentration in the electrolyte in the range from 1 to 10 ml/liter, and a plating suppressor having a concentration in the electrolyte in the range from 5 to 15 ml/liter.

14. The method as recited in claim 1 wherein the organic additives comprises a plating accelerator having a concentration in the electrolyte in the range from 1 to 10 ml/liter, a plating suppressor having a concentration in the electrolyte in the range

from 1 to 5 ml/liter, and a plating leveler having a concentration in the electrolyte in the range from 1 to 5 ml/liter.

15. The method as recited in claim 2 wherein the electropolishing and electroplating is performed using a nozzle configured to spray the wafer and to move form the wafer center to the wafer edge in a pass.

16. The method as recited in claim 2 wherein the electropolishing and electroplating is performed using a wafer-wide polisher.

17. The method as recited in claim 2 wherein each of the electropolishing, electroplating, and relaxation steps has a duration in the range from 1 to 100 ms.

18. An electrochemical polishing apparatus for performing electropolishing of a semiconductor substrate, the polishing apparatus configured to:

receive a substrate in an electrolyte plating solution having organic additives, the organic additives comprising at least one of plating accelerators, plating suppressors, and plating levelers; and

remove the excess portions of the metal layer by performing sequentially electrolytic polishing followed by electrolytic plating.

19. The apparatus as recited in claim 18 wherein the polishing apparatus is further configured to perform a relaxation step after the polishing and plating steps.

20. The apparatus as recited in claim 19 wherein the polishing, plating, and relaxation operations comprise one cycle of a pass and wherein the apparatus is further configured to perform at least two passes sequentially.